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**LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT**
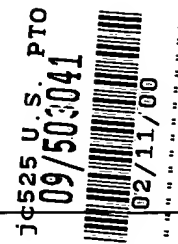
U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES	NO
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OTHER DOCUMENTS

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

K.E

1. S. Gupta, "Phase-Locked Loops," Proceedings IEEE, Vol. 63, pp. 291-306, February 1975.

2. W. Lindsey and C. Chie, "A survey of digital phase-locked loops," Proceedings IEEE, Vol. 69, pp. 410-432, 1981.

3. L. Franks, "Synchronization subsystems: analysis and design," Digital Communications, Satellite/Earth Station Engineering, K. Feher, ed.,, Prentice-Hall, Englewood Cliffs, NJ, pp. 294-325, 1981.

4. H. Meyr and G. Ascheid, "Synchronization in Digital Communications," New York, NY: Wiley Interscience, pp. 21-35, 1990.

5. J. Proakis, "Digital Communications," New York, NY: McGraw-Hill, 3rd ed., pp. 333-371, 1995.

6. A.J. Viterbi, "CDMA: Principles of Spread-Spectrum Communication," New York, Addison Wesley, Appendix 3A, pp. 68-75, 1995.

7. A. V. Oppenheim and R.W. Schafer, Digital Signal Processing, Englewood Cliffs, NJ, Prentice Hall, pp. 238-269, 1975.

8. J. L. Brenner, "Application of Chebychev Polynomials to Antenna Design," in Topics in Polynomials of One and Several Variables and their Application, T. M. Rassias, H.M. Srinivastava and A. Yanashaukas, editors, World Scientific Publ., pp. 101-108, 1993.

Examiner _[signature]_   Date Considered 5/1/03

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